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EXAMINER	
WASSUM, LUKE S	

ART UNIT	PAPER NUMBER
2177	13

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,316	BROOKLER ET AL.	
	Examiner	Art Unit	
	Luke S. Wassum	2177	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *64-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *64-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1 March 2004 has been entered.

Priority

2. The Applicants' claim to domestic priority under 35 U.S.C. §119(e) to provisional patent application 60/149,855, filed 19 August 1999, is acknowledged.

Drawings

3. On page 9 of the Applicants' submission, the Applicants state that they have submitted replacement sheets for Figures 3 and 10 as attachments in response to the examiner's drawing objections. However, the replacement sheets were not included with the Applicants' submission.

4. The drawing changes described on page 9 would satisfy the pending drawing objections, and are accepted as a proposed drawing correction. This proposed drawing correction is approved. Formal corrected drawings incorporating these proposed drawing changes are now required in reply to this Office action **in order to avoid abandonment of the application.**

The Invention

5. The claimed invention is a method of using bit vector indexes in order to increase the efficiency of database querying.

Claim Objections

6. In view of the cancellation of all pending claims, the claim objections are withdrawn.

Claim Rejections - 35 USC § 112

7. In view of the cancellation of the pending claims, the examiner withdraws the pending rejections under 35 U.S.C. § 112.

8. With regard to the Applicants' remarks that the 'logical AND' claim language is definite, the examiner responds that within the computer science art, the commonly accepted meaning of a logical AND operation is an operation wherein two Boolean expressions are each evaluated to 'true' or 'false', and then if both operands evaluate to true, then the result of the expression is true; if either or both of the operands evaluate to false, then the result of the expression is false.

In this application, the Applicants use the term 'logical AND operation' is used contrary to its commonly accepted meaning. The Applicants use this term to mean an operation wherein two expressions (bit patterns) are evaluated such that a bitwise AND operation is performed between them, and the resultant bit pattern is then evaluated as a Boolean, such that a positive result from the bitwise AND operation of any single bit will cause the result of the expression to be true; only if none of the bits evaluate positively will the resulting expression be false.

Nonetheless, in accordance with the MPEP § 2173.05(a) [R-1], terms used contrary to their ordinary meaning are allowed so long as the term is clearly redefined in the disclosure. The Applicants' description on pages 26-28, and Figures 9A and 9B fulfill this requirement. Therefore, the examiner finds that the pending claims satisfy the requirements of 35 U.S.C. § 112.

The examiner does note, however, that additional explanation of the Applicants' meaning of 'logical AND operation' in the claims, perhaps through an additional limitation or additional dependent claims, would serve to make the interpretation of the claims more clear.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 76 and 77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Regarding claim 76, the text of the claim seems to be intended to claim the embodiment of the invention wherein value limiting is performed, as disclosed in the specification beginning on page 24, line 17, and illustrated in drawing Figures 8, 9A and 9B. However, the specific matter claimed in claim 76 seems to be limited to a situation where there are only two possible values for the claimed 'first field', and furthermore the limitations regarding the calculation of 'counts', and the last limitation regarding 'having dimensions sized to a count regardless of the total data record

count' does not seem to have analogous disclosure, and the reason for the limitations and their purpose is unclear to the examiner.

The Applicants are requested to amend the claim to more clearly claim the embodiment as is disclosed in the specification and drawings, or alternately to provide sufficient explanation as to the correct claim interpretation so that the claim may be easily interpreted by one of ordinary skill in the art.

12. Claim 77, inheriting the deficiencies of its parent claim, is likewise rejected.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 64 and 65 are rejected under 35 U.S.C. 102(b) as being anticipated by **Wu et al.** ("Encoded Bitmap Indexing for Data Warehouses").

15. Regarding claim 64, **Wu et al.** teaches a method of indexing occurrences of a value in at least one data record using a bit vector as claimed, comprising:

a) associating a first bit vector with a first value to be held in a first field (see generation of bitmap vectors B_{Male} and B_{Female} in section 2.1 Simple Bitmap Indexing Revisited, page 2, and also Figure 1);

b) associating a second bit vector with a second value to be held in said first field (see associating a first bit vector with a first value to be held in a first field (see generation of bitmap vectors B_{Male} and B_{Female} in section 2.1 Simple Bitmap Indexing Revisited, page 2, and also Figure 1);

c) associating a first bit vector bit position from a plurality of bit vector positions in said first bit vector to a data record for each of a plurality of data records in a table (see disclosure that each bit is associated with a tuple, analogous to the claimed data record, section 2.1 Simple Bitmap Indexing Revisited, page 2);

d) associating a second bit vector bit position from a plurality of bit vector positions in said second bit vector to said data record for each of a plurality of data records in a table (see disclosure that each bit is associated with a tuple, analogous to the claimed data record, section 2.1 Simple Bitmap Indexing Revisited, page 2);

e) determining if said first value exists in said data record in said first field (see disclosure of the determination of whether GENDER=Male or GENDER=Female, section 2.1 Simple Bitmap Indexing Revisited, page 2);

f) determining if said second value exists in said data record in said first field (see disclosure of the determination of whether GENDER=Male or GENDER=Female, section 2.1 Simple Bitmap Indexing Revisited, page 2);

g) assigning a first Boolean value at said first bit vector bit position corresponding to said data record of said first bit vector corresponding to said first value based on said

determining if said first value exists step (see disclosure that the bit is assigned to zero or one depending upon whether GENDER equals Male or Female, section 2.1 Simple Bitmap Indexing Revisited, page 2);

h) assigning a second Boolean value at said first bit vector bit position corresponding to said data record of said second bit vector corresponding to said second value based on said determining if said second value exists step (see disclosure that the bit is assigned to zero or one depending upon whether GENDER equals Male or Female, section 2.1 Simple Bitmap Indexing Revisited, page 2);

i) accessing said first Boolean value from a bit vector index stored as an array comprising said first bit vector wherein said array comprises a first index accessed via said first value and a second index accessed by said first bit vector bit position (see discussion of the simple bitmap index on page 2, rendering the claimed method of updating bits upon changes to the data inherent, since without such updating the entire bitmap index would be rendered obsolete after the first data update, section 2.1 Simple Bitmap Indexing Revisited, page 2);

j) inverting said first Boolean value of said first bit vector corresponding to said first value at said first bit vector bit position to reflect a change of said first value to said second value in said data record in said first field (see discussion of the simple bitmap index on page 2, rendering the claimed method of updating bits upon changes to the data inherent, since without such updating the entire bitmap index would be rendered obsolete after the first data update, section 2.1 Simple Bitmap Indexing Revisited, page 2);

k) accessing said second Boolean value in said array comprising a second bit vector with said first index accessed by said second value and said second index accessed by said first bit vector bit position and wherein said first value and said second value comprise value limits of said first field (see discussion of the simple bitmap index on page 2, rendering the claimed method of updating bits upon changes to the data inherent, since without such updating the entire bitmap index would be rendered obsolete after the first data update, section 2.1 Simple Bitmap Indexing Revisited, page 2); and

l) inverting said second Boolean value of said second bit vector corresponding to said second value at said first bit vector bit position to reflect a change of said first value to said second value in said data record in said first field (see discussion of the simple bitmap index on page 2, rendering the claimed method of updating bits upon changes to the data inherent, since without such updating the entire bitmap index would be rendered obsolete after the first data update, section 2.1 Simple Bitmap Indexing Revisited, page 2).

16. Regarding claim 65, **Wu et al.** additionally teaches a method of indexing as claimed, further comprising encoding said bit vector into an encoded bit vector (see section 2.3 Encoded Bitmap Indexing, beginning on page 5).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. The factual inquiries set forth in *Graham* v. *John Deere Co*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

19. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

20. Claims 66 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wu et al.** ("Encoded Bitmap Indexing for Data Warehouses") as applied to claims 64 and 65 above, and further in view of **O'Neil et al. [1]** ("Improved Query Performance with Variant Indexes").

21. Regarding claims 66 and 67, **Wu et al.** teaches a method of indexing occurrences of a value in at least one data record using a bit vector substantially as claimed.

Wu et al. does not explicitly teach a method wherein encoding the bit vector comprises determining whether a frequency of a binary digit is less than a first threshold value, such as the number of bits used to store a number, and storing at least one position of said binary digit in said encoded bit vector.

O'Neil et al. [1], however, teaches a method further comprising encoding the bit vector representation by determining whether a frequency of a binary digit is less than the number of bits used to store a number, and storing as the encoded bit vector representation at least one position of the binary digit in the bit vector representation (see disclosure that when the disk space required to hold a bitmap column index is comparable to the disk space required for the RID-list index, the representation is changed from a bitmap to a RID list, a rowed being analogous to the claimed position of the bit, page 39, last paragraph of section 2.1.1 Bitmap Indexes).

It would have been obvious to one of ordinary skill in the art at the time of the invention to encode the bit vector in this way, since when average bitmap density for a bitmap index becomes too low, encoding the bit vector is more space efficient (see section 2.1.1 Bitmap Indexes, page 39).

22. Claims 68-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wu et al.** ("Encoded Bitmap Indexing for Data Warehouses") as applied to claims 64 and 65 above, and further in view of **O'Neil et al. [2]** ("Multi-Table Joins Through Bitmapped Join Indices").

23. Regarding claims 68-71, **Wu et al.** teaches a method of indexing occurrences of a value in at least one data record using a bit vector substantially as claimed.

Wu et al. does not explicitly teach a method wherein encoding the bit vector comprises compressing the bit vector by determining whether the size of a region of like binary digits is twice number of bits used to store a number, and storing as the encoded bit vector representation a representation of the region.

O'Neil et al. [2], however, teaches a method further comprising encoding the bit vector representation by compressing the bit vector by determining whether the size of a region of like binary digits is twice number of bits used to store a number, and storing as the encoded bit vector representation a representation of the region (see the disclosure regarding run-length encoding, page 9, last sentence of the last paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to change the manner of storage as claimed, since this would save in data storage, as disclosed in the last paragraph of page 9.

24. Claims 72 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wu et al.** ("Encoded Bitmap Indexing for Data Warehouses") in view of **Fulton et al.** (U.S. Patent 5,799,184).

25. Regarding claim 72, **Wu et al.** teaches a method of indexing occurrences of a value in at least one data record using a bit vector comprising:

a) associating a first bit vector with a first value to be held in a first field (see discussion of the concept of associating bit vectors to specific values held by specific fields, section 2.1 Simple Bitmap Indexing Revisited, beginning on page 2);

b) associating a second bit vector with a second value to be held in said first field (see discussion of the concept of associating bit vectors to specific values held by specific fields, section 2.1 Simple Bitmap Indexing Revisited, beginning on page 2);

c) associating a third bit vector with a third value to be held in a second field (see discussion of the concept of associating bit vectors to specific values held by specific fields, section 2.1 Simple Bitmap Indexing Revisited, beginning on page 2); and

d) performing a bit-level "OR" operation on said first bit vector with said second bit vector (see Cooperativity of Indexes, page 4, first two paragraphs, disclosing the efficiency of using simple bitmap indexes in conducting query operations).

Wu et al. does not explicitly teach a method of indexing wherein intermediate bit vectors are developed and used in subsequent bit-level operations.

Fulton et al., however, teaches a method of indexing wherein intermediate bit vectors are developed and used in subsequent bit-level Boolean operations (see col. 4, lines 14-19; see also col. 10, line 19 through col. 11, line 4).

It would have been obvious to one of ordinary skill in the art at the time of the invention to store intermediate bit vectors developed and use them in subsequent bit-level Boolean operations, since this would gain a distinctive advantage in speed and efficiency over conventional data search and retrieval systems by searching the more compact index files whenever possible to determine which data records satisfy specific search criteria (see col. 3, lines 14-19).

26. Regarding claim 73, **Fulton et al.** additionally teaches a method of indexing further comprising performing an operation with a new constraint to produce a second intermediate bit vector (see disclosure of the use of multiple intermediate bit vectors in solving a query, col. 10, lines 19-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to store intermediate bit vectors developed and use them in subsequent bit-level Boolean operations, since this would gain a distinctive advantage in speed and efficiency over conventional data search and retrieval systems by searching the more compact index files whenever possible to determine which data records satisfy specific search criteria (see col. 3, lines 14-19).

27. Claims 74 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wu et al.** ("Encoded Bitmap Indexing for Data Warehouses") in view of **Fulton et al.** (U.S. Patent 5,799,184) as applied to claims 72 and 73 above, and further in view of **Gupta et al.** ("Index Selection for OLAP").

28. Regarding claims 74 and 75, **Wu et al.** and **Fulton et al.** teach a method of indexing substantially as claimed.

Neither **Wu et al.** nor **Fulton et al.** explicitly teaches a method of indexing wherein the second intermediate bit vector is used as part of an ongoing iterative or interactive query.

Gupta et al., however, teaches a method of indexing wherein intermediate results (embodied in summary tables) are precomputed, stored and indexed for those subqueries which have been judged as being commonly requested, such as those that would be employed as part of an ongoing iterative or interactive query (see Abstract, page 208).

It would have been obvious to one of ordinary skill in the art at the time of the invention to precompute indexes for use in ongoing iterative or interactive queries, since this would reduce execution time for commonly requested queries (see Abstract, page 208; see also page 209, col. 1, first paragraph).

Response to Arguments

29. Applicant's arguments with respect to the newly added claims have been considered but are moot in view of the application of new prior art in rejecting these new claims.

30. The arguments regarding the interpretation of 'logical AND' and the claim rejections under 35 U.S.C. § 112 made as a result have been addressed above.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wu et al. (U.S. Patent 5,761,652) teaches a method of building balanced ranges of attribute values of multiple attributes which are then used to construct balanced range-based multidimensional bitmap indexes for processing complex multipredicate queries against the database.

Jakobsson et al. (U.S. Patent 5,848,408) teaches a method for processing star queries by utilizing one or more bitmap indexes built on columns of a fact table.

Cohen et al. (U.S. Patent 5,903,888) teaches a method for processing a query that uses a combination of different index types to minimize the rows of data that need to be retrieved from a table.

Cohen et al. (U.S. Patent 5,907,297) teaches a method for compressing bit indexes.

Jakobsson et al. (U.S. Patent 5,924,088) teaches the selection of indexes for an index access path that is based upon a cost/benefit analysis.

Ozbutun et al. (U.S. Patent 6,067,540) teaches a method for segmenting bitmaps in a bitmap index.

Ozbutun et al. (U.S. Patent 6,081,800) teaches a method for generating and using bitmaps in a database system that employs multi-level identifiers.

Ozbutun et al. (U.S. Patent 6,141,656) teaches a method for performing logical operations on bitmap streams from segmented bitmaps.

Feldman (U.S. Patent 6,154,741) teaches a method for determining accessor entitlement to a resource through the use of a membership map having membership information regarding the accessor and associates with the accessor a unique identifier that acts as an index into each membership map.

Bui et al. (U.S. Patent 6,285,994) teaches a method for efficiently searching an encoded vector index including the translation of a search query into a candidate bitmap and the mapping of data from the candidate bitmap into a search result bitmap according to entry values in the encoded vector index.

Chan et al. ("Bitmap Index Design and Evaluation") teaches a general framework to study the design space of bitmap indexes for selection queries and examines the disk-space and time characteristics that the various alternative index choices offer.

Datta et al. ("The DataIndex : A Structure for Smaller, Faster Data Warehouses") teaches the DataIndex, a family of design strategies for data warehouses to support OnLine Analytical Processing (OLAP).

Goyal et al. ("Indexing and Compression in Data Warehouses") teaches the application of compression techniques to data warehouses, particularly DataIndexes.

The following references, while not qualifying as prior art, is also of interest:

Ozbutun et al. (U.S. Patent 6,658,405) teaches a method for indexing a body of records, whereby the index associates ranges with records that hold key field values that fall within those ranges.

Wikipedia ("Logical Conjunction") teaches the definition of a 'logical AND' as it is commonly interpreted within the computer science art.

Wikipedia ("Bitwise Operation") teaches the definition of a 'bitwise AND' as it is commonly interpreted within the computer science art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke S. Wassum whose telephone number is 703-305-5706. The examiner can normally be reached on Monday-Friday 8:30-5:30, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Breene can be reached on 703-305-9790. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

In addition, INFORMAL or DRAFT communications may be faxed directly to the examiner at 703-746-5658.

Customer Service for Tech Center 2100 can be reached during regular business hours at (703) 306-5631, or fax (703) 746-7240.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luke S. Wassum
Art Unit 2177

lsw
7 April 2004